REMARKS

Claims 1, 3, 5-8, 10-12, and 16-20 are currently pending in the application, with claims 1 and 20 being independent. Claims 1, 3, 5-8, 10-12, and 16-20 were pending prior to the Office Action.

The Examiner is respectfully requested to reconsider the rejections in view of the amendments and remarks set forth herein. Applicant respectfully requests favorable consideration thereof in light of the amendments and comments contained herein, and earnestly seeks timely allowance of the pending claims.

Claim Rejections - 35 USC §102

The Examiner rejected claims 1, 3, 5 and 16-20 under 35 U.S.C. 102(b) as being anticipated by US 5,625,210 ("Lee et al.").

This rejection is respectfully traversed. Applicant respectfully submits the Examiner fails to establish a *prima facie* case of anticipation.

Lee et al. merely discloses an integration of two technologies (CMOS and CCD) wherein a pinned photodiode is integrated into the image sensing element of an active pixel sensor. Pinned photodiodes are fabricated with CCD process steps into the active pixel architecture. Charge integrated within the active pixel pinned photodiode is transferred into a charge sensing node by a transfer gate. The floating diffusion is coupled CMOS circuitry that can provide the addressing capabilities of individual pixels (Abstract).

Fig. 2 of Lee et al. illustrates a cross sectional diagram of the devices used in creating a sensor. An active pixel sensor (APS) architecture, typically fabricated in Complementary Metal Oxide Semiconductor (CMOS) technology, is integrated with a pinned photodiode 12 (PPD) device using a mixed process technology. The PPD 12 becomes the photoactive element in an XY-addressable area array with each pixel containing active devices for the transfer 14, readout via floating diffusion 16, and reset 18 functions (col. 2 lines 15-26).

As illustrated in Fig. 2 of Lee et al., the pinned photodiode 12 includes a pinning P+ layer 22 and a N+ implanted region 32 (col. 3 lines 25-27). A transfer section is formed using an N-

channel 14 and gate 24 having a connection TX (col. 3 lines 4-5). An NMOS transistor next to the transfer section includes an N+ source region 36, an N+ drain region connected to VDD, and a gate 24 connected to RESET. The source region 36 provides readout via floating diffusion to obtain an OUTPUT. Finally, a PMOS transistor is positioned at the far right in Fig. 2. N-well 40 (Fig. 2, col. 2 lines. 63-64) contains the PMOS transistor. The PMOS transistor includes a P+ source region, a P+ drain region and a gate 24. The pinned photodiode 22, the NMOS and the PMOS transistors are built on a P type epitaxial layer 4, which is located on a P type substrate 2 (Fig. 2).

In the sensor of Lee et al. illustrated in Fig. 2, charges are photo-generated in the photodiode 12. The charges are then transferred into the charge sensing node by transfer gate 14 (Abstract). A readout OUTPUT is obtained using the diffusion section 16. The NMOS can be reset using the RESET gate 24.

In Lee et al., the charge integrated within the active pixel pinned photodiode 12 in Fig. 2 are electrons generated in the N+ region 32, as described at col. 3 lines 19-25. Fig. 3f shows the construction of the PPD 12 by patterning with photoresist 56 areas for two additional implants. The first implant is to create a photodiode by implanting a deeper N+ impurity than was previously used by the source and drain implants discussed above. The deeper implant yields substantial increases in photo response due to an increase collection path for the incident photo carriers with the deeper implant. These electrons are then transferred along the N- channel 14 of the transfer gate, to N+ source region 36 of the NMOS, where they produce an OUTPUT signal.

In the Office Action (page 2), the Examiner asserted that the right half of rightmost N+ region in Fig. 2 is allegedly a charge accumulation region. However, this region is not a charge accumulation region for which a signal potential that changes in accordance with the amount of the charges in the charge accumulation region, is caused to be generated as an image signal, as claimed in claims 1 and 20. In the sensor of Lee et al., output signals are obtained from the source region 36, along the line labeled OUTPUT in Fig. 2. Hence, output signals are generated by charges in the N+ source region 36, and not by charges in the rightmost N+ region (drain region connected to VDD).

The Examiner also asserted on page 2 of the Office Action that the channel region beneath the gate of the RESET transistor having gate 24 is allegedly a charge transfer region. As discussed above, the right half of rightmost N+ region in Fig. 2 of Lee et al. is not a charge accumulation region as claimed in claims 1 and 20. The channel region beneath the gate of the RESET transistor having gate 24 is therefore not provided between a charge generating region and a charge accumulation region of the pixel, because charges are generated in the photodiode 12 (left of the channel region beneath the gate of the RESET transistor having gate 24), but a charge accumulation region is not found at the right of the channel region beneath the gate of the RESET transistor. Hence, the channel region beneath the gate of the RESET transistor is not a charge transfer region as claimed in claims 1 and 20.

Lee et al. does not disclose a first charge eliminating region formed between a substrate and a charge accumulation region, the first charge eliminating region forming a second potential barrier to the charges in the charge accumulation region, the second potential barrier being removable according to an applied voltage to the first charge eliminating region, as claimed in claims 1 and 20.

In the Office Action (page 2), the Examiner asserted that the epitaxial layer 4 of Lee et al. is allegedly a first charge eliminating region. However, the epitaxial layer 4 does not form a second potential barrier to the charges in the right half of rightmost N+ region in Fig. 2, or to the charges in the N+ region 36, the second potential barrier being removable according to an applied voltage to the epitaxial layer 4.

The charges accumulated in the N+ region of the NMOS are electrons, while the epitaxial layer 4 is a P-type layer. Hence, the interface between any of the N+ NMOS regions and the P type epitaxial layer 4 is an NP junction. During operation of the sensor of Lee et al., this junction is not allowing the photo-generated electrons to go to the P type epi layer 4, since it is clear from Lee et al. that photo-generated electrons are localized first in the N+ well 32, then in the N+ region 36, and are then eliminated through the NMOS drain region, by a reset operation controlled by the RESET gate 24. The RESET gate is a gate of the NMOS transistor and only

controls a channel formed horizontally between the N+ region 36 and the drain N+ region connected to VDD.

Hence, the P type epi layer 4 of Lee et al. is a barrier to electrons in the N+ regions. This barrier is not removable according to an applied voltage to the epi layer 4, for the following reasons. The right half of rightmost N+ region in Fig. 2 is not a charge accumulation region, as explained above. Hence, the portion of the P type epi layer 4 located below the right half of rightmost N+ region in Fig. 2 is not a first charge eliminating region formed between the substrate and a charge accumulation region.

Moreover, the portion of the P type epi layer 4 located below the N+ region 36 does not form a second potential barrier being removable according to an applied voltage to the epi layer 4. That is because the NP junction between the N+ region 36 and the P epi layer 4 is a barrier to electrons as explained above. This NP junction cannot become a free path for electrons, because no biasing voltage connections are made to the P layer 4 or to the N+ region 36. No biasing voltage connection for the P epi layer 4 is discussed anywhere in Lee et al. Furthermore, the only connection to the N+ region 36 is the OUTPUT line illustrated in Fig. 2. No biasing voltage connection is illustrated on that OUTPUT line, for biasing an NP junction between the N+ region 36 and the P epi layer 4. No biasing voltage connection is discussed anywhere in Lee et al. along the OUTPUT line, for biasing the NP junction between the N+ region 36 and the P epi layer 4 to a conductive mode.

Hence, the epi layer 4 will present a non-removable barrier to electrons.

Lee et al. also does not disclose a solid-state imaging device in which when a first and second potential barriers are removed, the charges which have been accumulated in a charge generating region are eliminated to the substrate through the charge accumulation region before starting accumulation of the charges in the charge generating region, as claimed in claims 1 and 20. The barrier posed by the P epi later 4 is a non-removable barrier to electron charges, and it is impossible for electrons from the N+ region of the NMOS to reach the substrate 2. Furthermore, charges in the sensor of Lee et al. are eliminated through the leads attached to the N+ regions of the NMOS, and not through the substrate 2.

Lee et al. also does not disclose a second charge eliminating region formed near the charge generating region as claimed in claims 1 and 20.

In the Office Action (page 3), the Examiner asserted that the pinning layer 22 is allegedly a second charge eliminating region.

However, in Lee et al., the pinning layer 22 - which is a P+ layer - cannot eliminate photo-generated electrons anywhere. The P+ pinning layer 22 contains holes and represents a barrier to electrons from the N+ well 32. Moreover, the P+ pinning layer 22 is surrounded by isolation oxide/field oxide on the top and left side (the layer covering the top of the structure in Fig. 2, col. 2 lines 66-67), and by the N+ well 32 on the bottom. Oxide is non-conducting, and electrons cannot be eliminated through the oxide. Hence, the pinning layer 22 cannot eliminate photo-generated electrons from the N+ well 32 to anywhere.

During operation of the sensor of Lee et al., electrons are photo-generated in the photodiode 22 N+ well 32. These electrons are clearly not eliminated at that time by the pinning layer 22. The voltage potential configuration of the junction formed at the pinning layer 22 and the N+ well 32 is never changed to move electrons from the N+ well 32 to the P+ pinning layer 22, because there are no biasing voltage contacts contacted to the N+ well 32 or to the P+ pinning layer 22. The pinning layer 22 is covered by an oxide layer throughout. Hence, no biasing voltages can be applied to the P+ pinning layer 22, and the PN junction between the N+ well 32 and the P+ pinning layer 22 cannot become biased for any elimination of electrons through layer 22.

Therefore, the pinning layer 22 is not a charge eliminating region.

With respect to claim 20, Lee et al. also does not disclose a region, provided between a charge generating region and an overflow drain region, that forms a third potential barrier to the charges in the charge generating region, the third potential barrier being lower than a first potential barrier such that the charges that are overflowed from the charge generating region are eliminated via the second charge eliminating region.

In the Office Action (page 4), the Examiner asserted that transfer 14 is allegedly such a region, and that N+ section 36 is an overflow drain region. However, the N+ section 36, which is

the source of the NMOS, produces an output readout of the charge, and does not process a charge overflow. Charge overflows and handling of charge overflows are not discussed anywhere in Lee et al.

Furthermore, Lee and al. does not discuss any third potential barrier which would be lower than a first potential barrier such that charges that are overflowed from the photodiode 32 are eliminated via a second charge eliminating region. As pointed out earlier, the right half of rightmost N+ region in Fig. 2 is not a charge accumulation region, and the channel region beneath the gate of the RESET transistor having gate 24 is not a charge transfer region provided between a charge generating region and a charge accumulation region. The channel region beneath the gate of the RESET transistor is not a charge transfer region which forms a first potential barrier to the charges in a charge generating region. Hence, no first and third potential barriers, the third potential barrier being lower than the first potential barrier, exist in Lee et al.

The sensor of Lee et al. is in fact adapted to function in a completely different manner than the solid-state imaging device of claims 1 and 20. In the sensor of Lee et al., electrons are generated in the photodiode 22, transferred to the N+ well 36 for readout, and eliminated by reset 18 of the NMOS. The sensor of Lee et al. does not have and does not use a first charge eliminating region formed between the substrate and a charge accumulation region, the first charge eliminating region forming a second potential barrier to charges in the charge accumulation region, the second potential barrier being removable according to an applied voltage. The sensor of Lee et al. also does not have and does not use a second charge eliminating region formed near a charge generating region. Furthermore, in the sensor of Lee et al., first and second potential barriers are not removed, and charges which have been accumulated in the charge generating region are not eliminated to the substrate through the charge accumulation region before starting accumulation of the charges in the charge generating region. The sensor of Lee et al. is not adapted to function like the solid-state imaging device of claims 1 and 20.

To the extent that the Examiner is ignoring or not giving proper weight to functional limitations in the claims, please consider the case law listed below regarding functional limitations.

Functional definitions are not only common but have been expressly approved in many cases including *Locklin et al. v. Switzer Bros., Inc.*, 299 F.2d 160, 131 USPQ 294 (C.A. 9th); *Sales Affiliates, Inc. v. Hutzler Bros. Co.*, 71 F.Supp. 287, 72 USPQ 211 (D.C. Md), at 216, aff'd., 164 F.2d 260, 75 USPQ 259 ; *Ex parte Sperr*, 12 USPQ 194 (PO Bd.); *Ex parte Carter*, 52 USPQ 186 (PO Bd.); *Ex parte Kellog*, 84 USPQ 380 (PO Bd.); and *Ex parte Ebel and Drew*, 84 USPQ 202 (PO Bd.). Also, analogous "functional" limitations with respect to uncritical time or temperature have been approved in claims in: *Ex parte Ebel and Drew, supra*; *Ex parte Fowler and Otis*, 46 USPQ 425 (PO Bd.); *Procter & Gamble Mfg. Co. v. Refining, Inc.*, 135 F.2d 900, 57 USPQ 505 (C.A. 4th); and *Ex parte Clarke*, 98 USPQ 195 (PO Bd.).

It is well established that functional elements should be considered in claim analysis. In *Clements Industries Inc. v. A. Meyers & Sons Corp.*, 12 USPQ2d 1874 (SD NY 1989), the Court stated "We are aware that functional language such as that here at issue ... is allowed in claims and is entitled to full weight in claim analysis" citing to *In re Swinehart and Sfiligoj*, 169 USPQ 226 (CCPA 1971).

Accordingly, Applicant respectfully requests the Examiner to give all of the claim features patentable weight and due consideration in accordance with the above cited case law.

Hence, with respect to claim 1, Lee et al. fails to disclose, at least, "a first charge eliminating region formed between the substrate and the charge accumulation region, the first charge eliminating region forming a second potential barrier to the charges in the charge accumulation region, the second potential barrier being removable according to an applied voltage to the first charge eliminating region, and when the first and second potential barriers are removed, the charges which have been accumulated in the charge generating region are eliminated to the substrate through the charge accumulation region before starting accumulation of the charges in the charge generating region, and then upon formation of at least the second potential barrier, the charges start to be generated by light irradiation to the charge generating region, to accumulate the charges in the charge accumulation region, and wherein formation of the first potential barrier after a predetermined time of the light irradiation prevents the charges that are generated by the light irradiation to the charge generating region from being transferred

to the charge accumulation region, and then causes a signal potential that changes in accordance with the amount of the charges in the charge accumulation region to be generated as an image signal, a second charge eliminating region formed near the charge generating region, wherein the second charge eliminating region is a p + type impurity region formed on an upper surface of an n + type impurity region in the photo diode."

Also, with respect to claim 20, Lee et al. fails to disclose, at least, "a first charge eliminating region formed between the substrate and the charge accumulation region, the first charge eliminating region forming a second potential barrier to the charges in the charge accumulation region, the second potential barrier being removable according to an applied voltage to the first charge eliminating region, and when the first and second potential barriers are removed, the charges which have been accumulated in the charge generating region are eliminated to the substrate through the charge accumulation region before starting accumulation of the charges in the charge generating region, and then upon formation of at least the second potential barrier, the charges start to be generated by light irradiation to the charge generating region, to accumulate the charges in the charge accumulation region, and wherein formation of the first potential barrier after a predetermined time of the light irradiation prevents the charges that are generated by the light irradiation to the charge generating region from being transferred to the charge accumulation region, and then causes a signal potential that changes in accordance with the amount of the charges in the charge accumulation region to be generated as an image signal, and further comprising: a second charge eliminating region formed near the charge generating region, a region, provided between the charge generating region and an overflow drain region, that forms a third potential barrier to the charges in the charge generating region, the third potential barrier being lower than the first potential barrier such that the charges that are overflowed from the charge generating region are eliminated via the second charge eliminating region."

For all of the above reasons, taken alone or in combination, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. 102 (b) rejection of claims 1 and 20.

Claims 3, 5 and 16-19 depend from claim 1 and are allowable at least by virtue of their dependency.

Claim Rejections - 35 USC §103

The Examiner rejected claims 6 and 7 under 35 U.S.C. 103 (a) as being unpatentable over Lee et al. in view of US 6,476,371 ("Miida").

Applicant traverses this rejection. Applicant respectfully submits the Examiner has failed to establish a *prima facie* case of obviousness.

Applicant submits that the Examiner's reliance on Miida on page 6 of the Office Action as allegedly pertaining to incremental features of claims 6 and 7 fails to make up for the deficiencies of the asserted Lee et al. reference discussed above with respect to independent claim 1. Therefore, the asserted grounds of rejection fail to establish *prima facie* obviousness of any pending claim.

The teachings of Lee et al. are presented above in the arguments traversing the §102 rejections of claims 1 and 20. As provided above in the arguments for the allowability of claim 1, Lee et al. fails to teach or suggest all of the elements for claim 1.

For all of the above reasons, taken alone or in combination, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. 103 (a) rejection of claims 6 and 7.

Election Requirement

The Examiner has made the Restriction Requirement final and has withdrawn claims 10-13 from consideration. Claim 13 was previously cancelled. Assuming independent claim 1 is found to be allowable, it is respectfully requested that the Examiner also consider and allow withdrawn claims 10-12.

If the Examiner persists in this Restriction Requirement, the Applicant reserves the right to file one or more divisional applications at a later date if so desired.

CONCLUSION

In view of the above amendments and remarks, this application appears to be in condition for allowance and the Examiner is, therefore, requested to reexamine the application and pass the claims to issue.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Corina E. Tanasa, Limited Recognition No. L0292 under 37 CFR §11.9(b), at telephone number (703) 208-4003, located in the Washington, DC area, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly extension of time fees.

Dated: September 6, 2007

Respectfully submitted,

By _____

Michael R. Cammarata
Registration No.: 39,491
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East, P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

MRC/CET